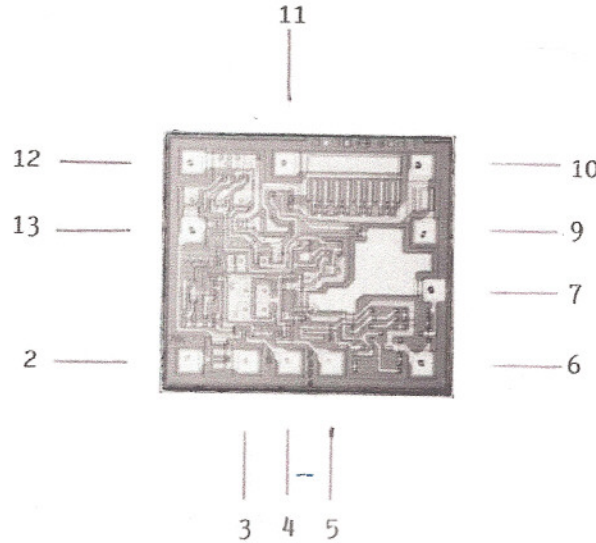




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**PIN/PAD FUNCTION:**

- |               |                 |
|---------------|-----------------|
| 1. N.C.       | 9. $V_Z$        |
| 2. b          | 10. $V_0$       |
| 3. e          | 11. $V_C$       |
| 4. -IN        | 12. $V_{CC}^+$  |
| 5. +IN        | 13. Freq. Comp. |
| 6. $V_{REF}$  | 14. N.C.        |
| 7. $V_{CC}^-$ | 15.             |
| 8. N.C.       | 16.             |

**APPROVED BY:MG**

**DIE SIZE :50 x 45 mils**

**DATE: 12/17/08**

**MFG:CSF THOMPS**

**THICKNESS:**

**P/N:UA723**